Energy Efficient System Design

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Designing low power and energy efficient computing and communication systems needs a holistic approach from system to circuit and below.

System Level:
• Probabilistic design with QoS guarantee
• Parallelism in multi-core systems
• Heterogeneous and reconfigurable system
• Fault tolerant systems

Application Level:
• Real-time task/job scheduling
• Dynamic voltage and frequency scaling
• Energy aware computing
• Approximate computing

Logic Level:
• FSM re-engineering and re-encoding
• Gate replacement and logic reconstruction

Approaches:
• Dual-Vt design
• Input vector control for leakage reduction
• Temperature aware computing

Cross layer:
• Computation vs communication
• Energy harvesting and scavenging

Applications
• Real-time Embedded Systems
• Internet of Things (IoTs)
• Green Computing and Communication
• Portable Devices
• Wearable/Implantable Medical Devices
• Wireless Sensor Networks

Future Work
• Approximate Computation
• Low Power Memory Design
• Improved DVFS techniques
• Energy harvesting
• Energy aware computing

Our Solution:
Simultaneous assignment algorithm

Dual Voltage & Frequency Scaling
Circuits can work at a range of $V_{dd}$ values. Reduce $V_{dd}$ to $\gamma V_{dd}$

Motivation:
Low Power designs should consider temperature variations.

Problem:
• Given current temperature and maximum temperature what is the maximum workload can be done by a DVS processor?
• How to design temperature aware dual-Vt systems?

Solution:
• Temperature aware leakage minimization algorithm.
• Temperature aware dual-Vt design
• All-DVS algorithm

Temperature aware design

Before temperature aware optimization:
• Peak temperature: 70.54°C
  • 1309 cells in 55.37°C

After temperature aware optimization:
• Peak temperature: 68.54°C
  • 863 cells in 55.37°C or higher

Dual Threshold Voltage $V_t$ Design
Goal: Reduce leakage power
Approaches:
• Use minimum leakage vector (MLV) for sleep
• Use dual $V_t$ design:
  -- high $V_t$ for low leakage
  -- low $V_t$ for critical path

Challenges:
• Interdependency between input vector and dual $V_t$ assignments.
• Simultaneous optimization required

Circuits Level:
• Approximate computing

Logic Level:
• FSM re-engineering and re-encoding
• Gate replacement and logic reconstruction

FSM reengineering
Goal: Reduce switching activity in a circuit to reduce dynamic power.

Method: Re-constructs a minimized FSM and re-encodes it to achieve better synthesis solutions with low power.

Future Work
• Approximate Computation
• Low Power Memory Design
• Improved DVFS techniques
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Probabilistic Design
Application area:
• multimedia embedded systems

Why:
• These systems are overdesigned.
• Uncertainties in execution time.
• Tolerance for execution failures.