Advanced CMOS Imaging

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Introduction

Image sensors convert optical images into electric signals and are one of the most prevalent sensors in use today due to their unrivaled

- Massively parallel data acquisition
- Sensitivity
- Selectivity

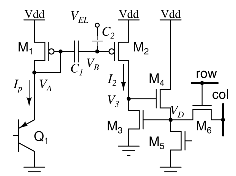
CMOS image sensors have several advantages over other imaging sensors:

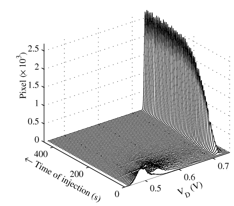
- Ease of integration with other electronics
- Integrated signal processing
- Low cost
- Compatibility with lab-on-a-chip (LOC) systems

Our lab has developed specialized CMOS imagers with a focus on biosystems applications such as lab-on-a-chip systems, image plane processors, flight stabilization for unmanned aerial vehicles, and medical diagnostics.

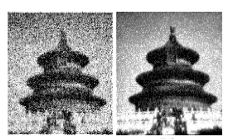
Specialized sensors include imagers optimized for: low light detection, low noise detection, pattern classification, mismatch compensation, feature extraction, photon counting, high energy radiation detection, as well as others.

Adaptive Floating Gate Imager



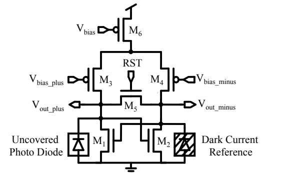


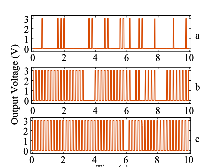
- Novel adapting current mode imager automatically removes fixed pattern noise (FPN) from all pixels simultaneously.
- Floating gates store corrective charge locally in each pixel.
- The pixel exploits the negative feedback mechanism of pFET hot-carrier injection.
- Floating gate adaptation reduces noise power 100 times at the calibration intensity and 10 times over 5 orders of magnitude of intensity.



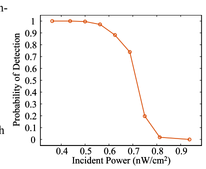
(a) Before (b) After

Optical Comparator

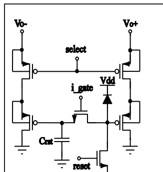




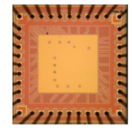
- The sensor is comprised of a clocked comparator with enlarged drain-substrate n^+-p_{sub} junctions acting as photodiodes.
- One of the photodiodes is covered with metal to provide a dark current reference, and the bias current is varied to set the detection threshold.
- Changes in illumination due to a rotating fan blade at 100 Hz were successfully detected.
- Results support application to particle detection and localization with 1- bit resolution (i.e., optical threshold crossing).



Differential APS

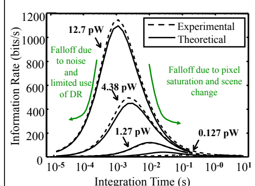


- Differential structure mitigates correlated noise at expense of moderate increases in fundamental reset noise and readout noise
- Offers a good design tradeoff for many applications, including small portable imaging systems



	Total Reset	Fund. Reset	Total Readout	Fund. Readout
Single	0.65 mV	0.12 mV	1.15 mV	0.13 mV
Differential	0.46 mV	0.36 mV	0.13 mV	0.17 mV
Reduction	1.4 X ↓	3 X ↑	9.2 X ↓	1.4 X ↑

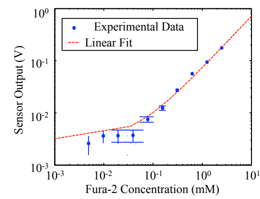
Rejection of Correlated Noise Sources



- Information rate for charge mode image sensor determined as a function of integration time and optical power:

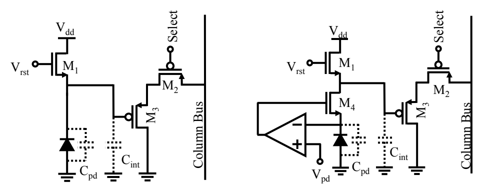
$$R = \frac{1}{2t_{int}} \log_2 \left[1 + \frac{6}{\pi e} \frac{\frac{\sigma_s^2 I_{ph}^2 t_{\mathrm{int}}^2}{C_{\mathrm{int}}}}{V_{n_{rst}}^2 + V_{n_{shot}}^2 + V_{n_{rdout}}^2} \right]$$

- For each intensity, the maximum information rate corresponds to a unique integration time



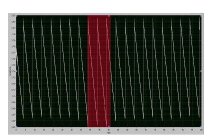
- Measured detector sensitivity to Fura-2 in calcium free buffer
- Fura-2 is a common calcium indicator
- Accurately measured concentrations of Fura-2 from 5uM to 39 nM
- "Accurately" = signal at least one standard deviation above noise floor

Low Dark Current APS

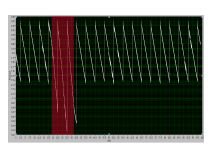


Standard 3-transistor APS Element **Modified LNAPS Element**

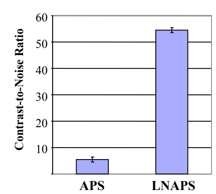
- Standard APS with three transistor elements, used to reset, buffer the photodiode, and to select the pixel element for readout.
- Low Noise APS (LNAPS) with feedback loop that clamps the photodiode voltage near zero and isolates the integration node from the parasitic capacitance of the photodiode, increasing the front-end gain.



Standard 3-transistor APS experiment: 75KeV X-ray dose applied between times 35-37s highlighted in red



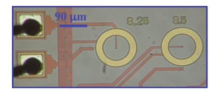
Now-noise APS experiment: 75KeV X-ray applied between times 18-30s, highlighted in red

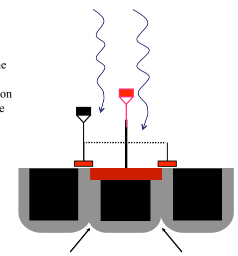


- LNAPS provides 10X increase in contrast-to-noise ratio.

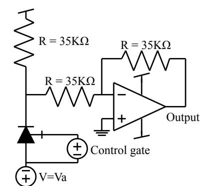
Single Photon Avalanche Diodes

- Motivation: Perimeter breakdown and high dark count rates are the primary challenges to implementing single photon avalanche diodes (SPADs) in a standard CMOS process.
- Approach: a control gate placed over the perimeter of the junction effectively suppresses perimeter breakdown while suppressing dark count. In addition, lateral diffusion of n-wells is used to further improve device performance by reducing the built-in electric field at the edge of the structure.

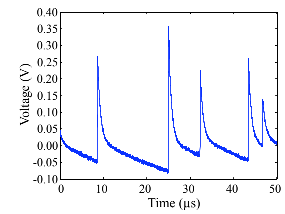




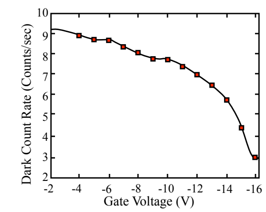
Lateral N-well Diffusion – Perimeter breakdown suppression



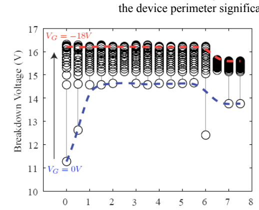
Passive quenching circuit for SPAD using off-chip quenching resistors achieves a timing resolution of 500 ns.

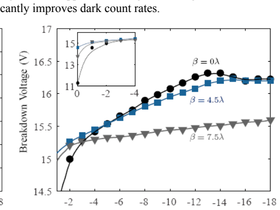


Transient trace of dark events occurring in a SPAD structure with 6 lambda N-well spacing



Dark count rate as a function of gate voltage. Field suppression using a control gate at the device perimeter significantly improves dark count rates.





- Breakdown voltage as a function of N-well spacing and gate voltage.
- With no gate bias, breakdown is higher for intermediate N-well spacing.
- Each vertical line shows how control gate bias voltage affects breakdown for a specified value of N-well spacing.

- Breakdown voltage as a function of gate voltage, for three different N-well spacings.

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