Faster CMOS Inverter Switching Obtained with Channel Engineered Asymmetrical Halo Implanted MOSFETs

Akin Akturk, Neil Goldsman, George Metze†

Department of Electrical and Computer Engineering, University of Maryland, College Park, MD 20742, USA
†Laboratory of Physical Sciences, College Park, MD 20742, USA
akturka@glue.umd.edu, neil@eng.umd.edu, metze@eng.umd.edu

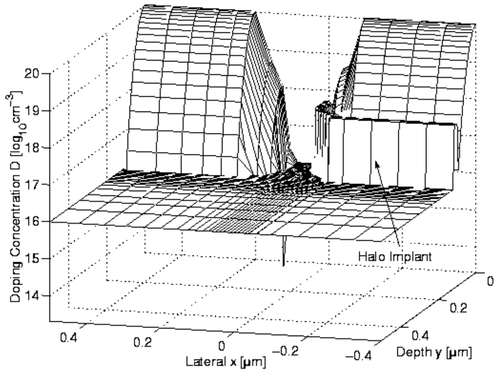
Semiconductor Device and Circuit Laboratory

Design Methodology

The methodology is to optimize the channel doping such that the device performance is improved.

We replaced the highly doped substrate with a lightly doped substrate, that is supplemented with a highly doped halo implant around either the source or drain.

- **To achieve the S/D isolation using smaller amounts of dopants**
- **To keep the threshold value same for the whole device but lowering it outside the halos**
- **To decrease the channel on-resistance by easing the channel inversion through the lightly doped channel region**
- **To lower junction capacitances by removing the unnecessary bulk for the device operation**
- **To effectively have a smaller device, which is the halo region in the channel instead of the whole channel**



Doping Profile of a 0.1μm Physical Gate Length Source Side Halo Implanted NMOSFET

Devices	D_{SUB} (cm^{-3})	D_{HALO} (cm^{-3})
Halo	$1x10^{16}$	$5x10^{17}$
Conventional	$5x10^{17}$	-

DHM ——— Drain halo implanted
SHM — — — Source halo implanted
CM - - - - - - - - Conventional
Legend

Mixed-Mode Simulator

DD Equations

$$\nabla^2\phi = -\frac{q}{\varepsilon_{Si}}(p - n + D)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla.\overrightarrow{J_n} - R_n + G_n$$

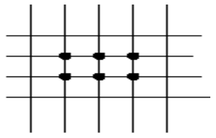
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla.\overrightarrow{J_p} - R_p + G_p$$

Supplementary DD Equations

$$\overrightarrow{J_n} = -q\mu_n n\overrightarrow{\nabla\Phi} + q\mu_n V_T\overrightarrow{\nabla n}$$

$$\overrightarrow{J_p} = -q\mu_p p\overrightarrow{\nabla\Phi} - q\mu_p V_T\overrightarrow{\nabla p}$$

Coupled Discretized DD Equations are solved at each mesh point. There are about 40x40 mesh points.

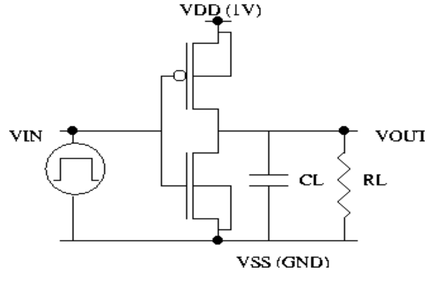


Lumped KCL equation check at the output node and using the KCL equation, the output guess is updated for the next iteration, V_O^{i+1}:

$$I_{DN} - I_{DP} + I_{R_L} + I_{C_L} = 0$$

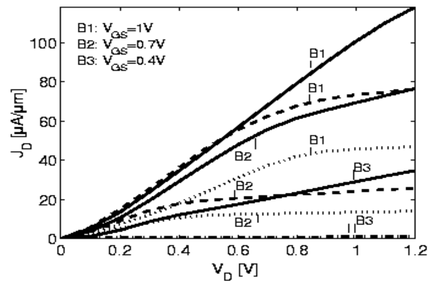
$$A_N + B_N V_o^{i+1} + A_P + B_P V_o^{i+1} + \frac{V_o^{i+1} - V_{SS}}{R_L} + C_L\frac{V_o^{i+1} - V_o^i}{\Delta t} = 0$$

$$V_o^{i+1} = \frac{V_{SS} + V_o^i\frac{R_L C_L}{\Delta t} - (A_N + A_P)R_L}{1 + \frac{R_L C_L}{\Delta t} + (B_N + B_P)R_L}$$

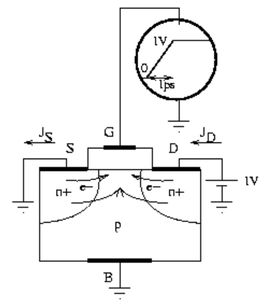


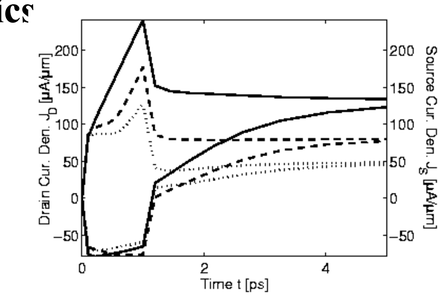
CMOS Inverter

NMOS Characteristics



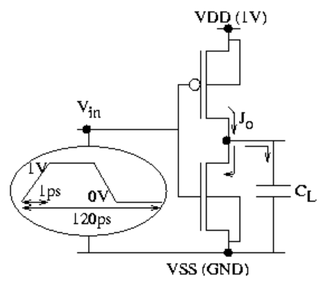
NMOS DC Current Densities, V_{SB}=0V

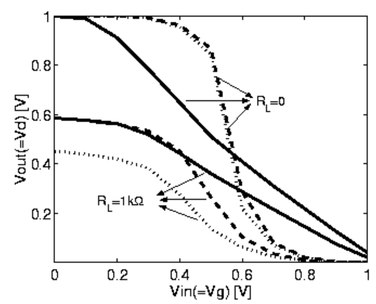


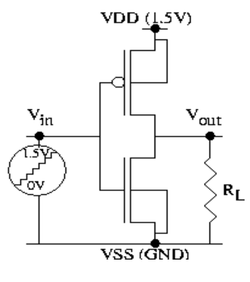


NMOS Turn-on

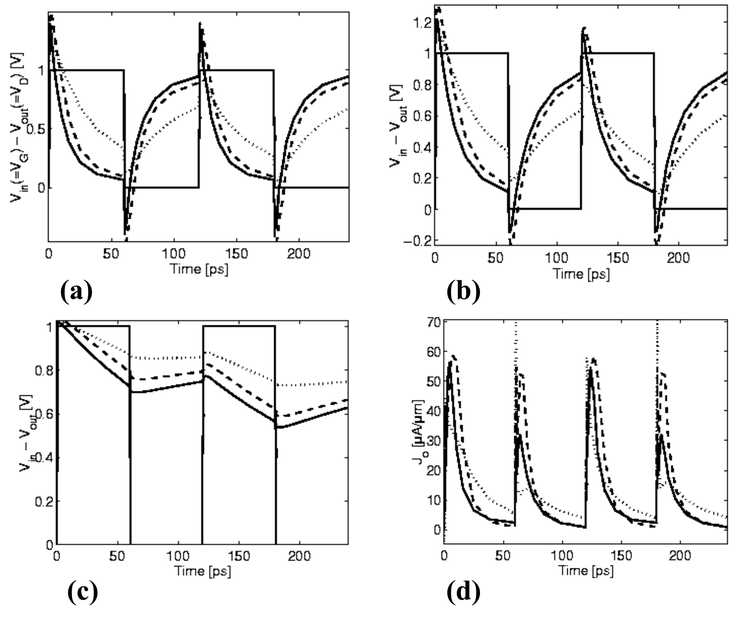
CMOS Inverter Characteristics







Transfer Characteristics of CMOS Inverters with(out) a Resistive Load.



Switching Characteristics of CMOS Inverters (a) without a Capacitive Load (C_L), with C_L (b) 10fF and (c) 0.3pF. The output current densities are also shown in (d) for the CMOS Inverters without C_L.

Conclusion

- **A novel algorithm is developed to make the transient analysis of the CMOS Inverters.**
- **Halo implanted devices have**
  - **Lower channel on-resistance, so have higher drive currents**
  - **Reduced internal capacitances; junction capacitances**
- **The inverters utilizing the halo implanted devices have**
  - **Faster switching speeds**
  - **Better current supplying capabilities**
- **DHM**
  - **Has the highest drive currents.**
  - **Suffers from DIBL, so leakage is a problem and should be compensated for**
  - **Has low output resistance**
  - **Results in the fastest switching if used in CMOS Inverters**
- **SHM**
  - **Has high output resistance**
  - **Supplies more current to the load if used in the CMOS Inverter**
  - **Has the biggest voltage swing in inverter configuration**