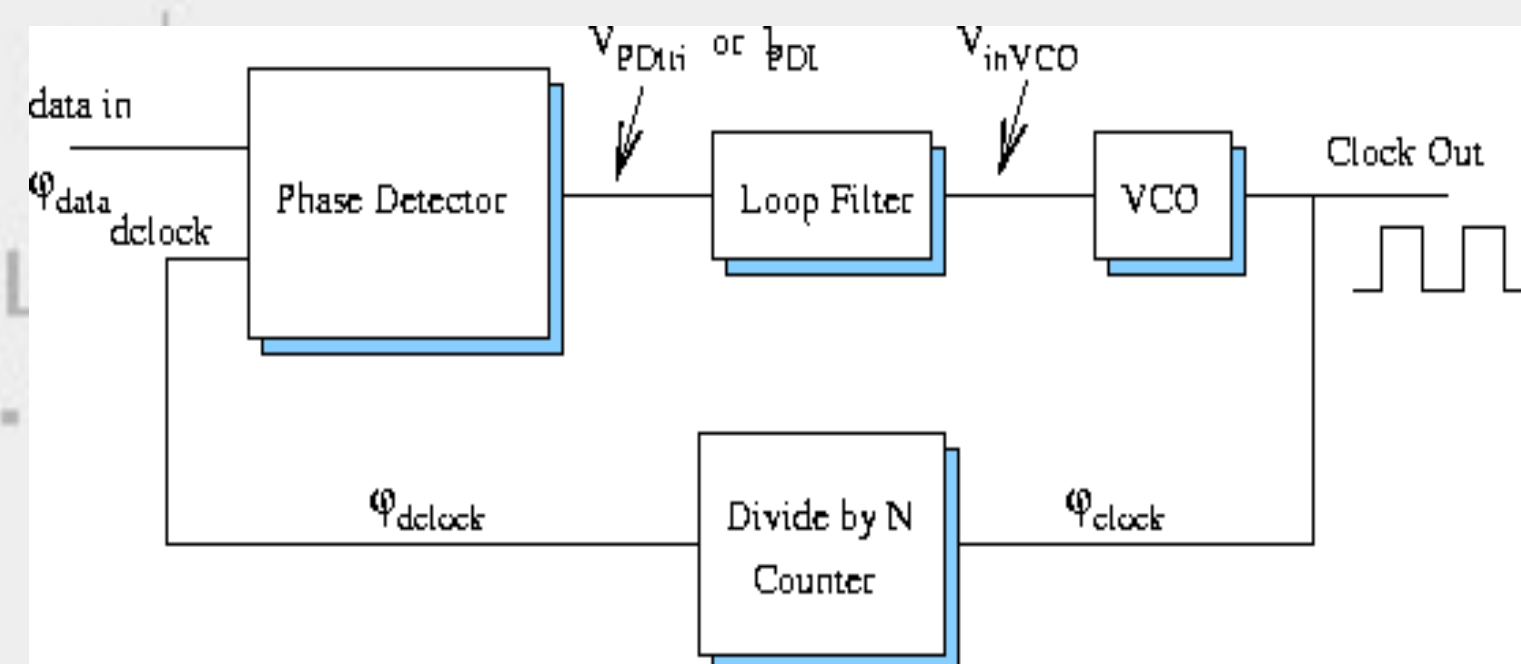


# Phase-Locked Loop Design

Akin Aktürk, Zeynep Dilli, Neil Goldsman

## Phase-Locked Loops

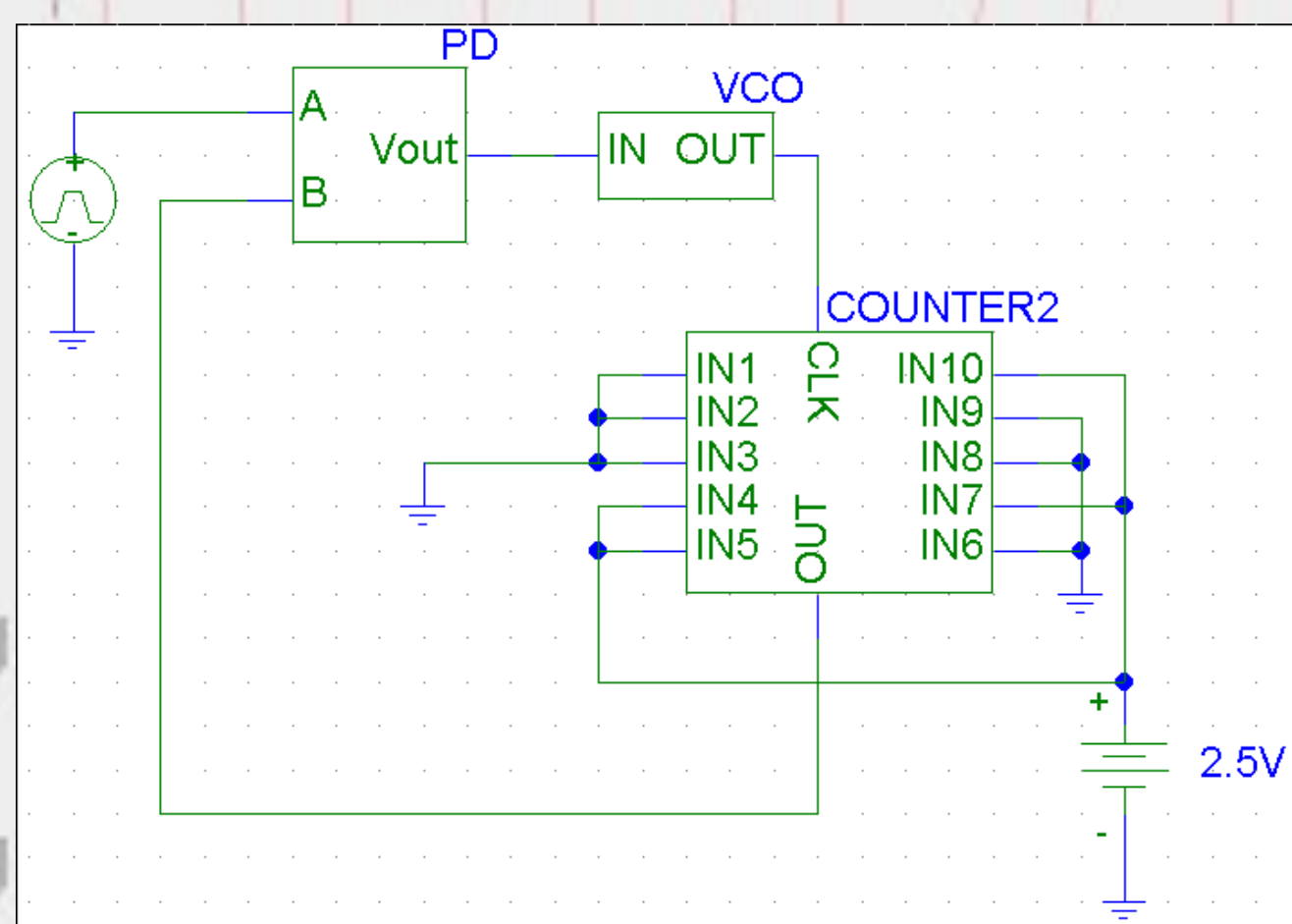
- Phase-locked loops: Building blocks in receivers and other communication electronics
- Main premise: Lock in to a frequency or phase component of an incoming signal and give a synchronized output
- Block diagram:



## Design Specifications

- Design Goal** Given a reference clock signal at 200 kHz, design a PLL whose output will oscillate in a range between 110 MHz to 130 MHz.
- For the block diagram above, this requires a divide-by-N counter with N between 550 and 650.
- Therefore we used a 10-bit binary downcounter. The inputs set the number it starts counting down from. The output of the VCO is the "count" signal for the counter. When the counter reaches zero, it is reloaded and sends a pulse to the phase detector.

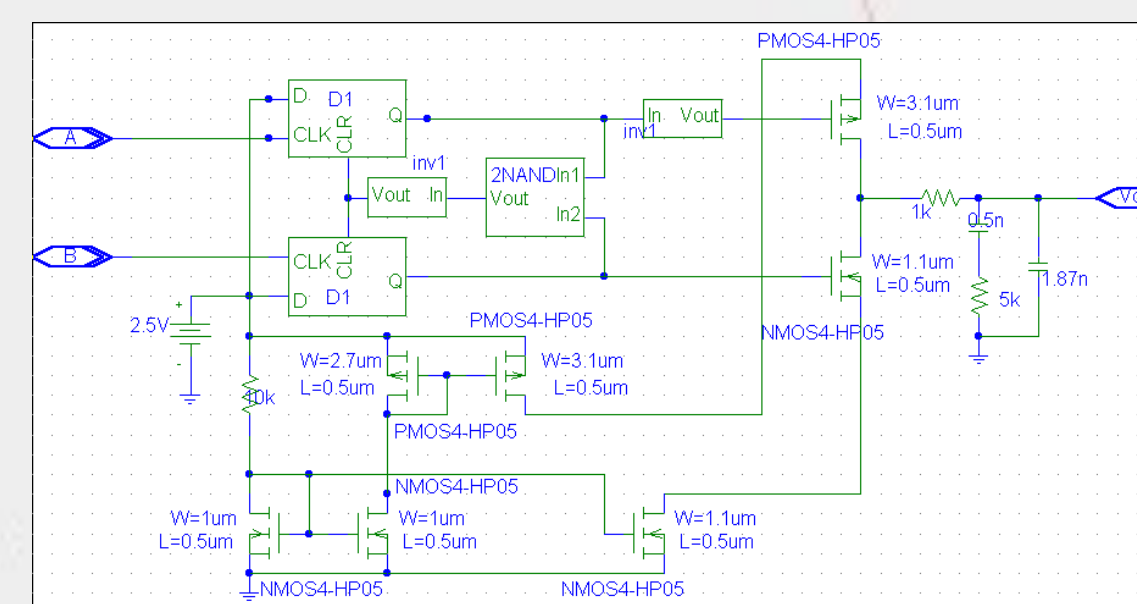
## Phase-Locked Loop, Complete Circuit



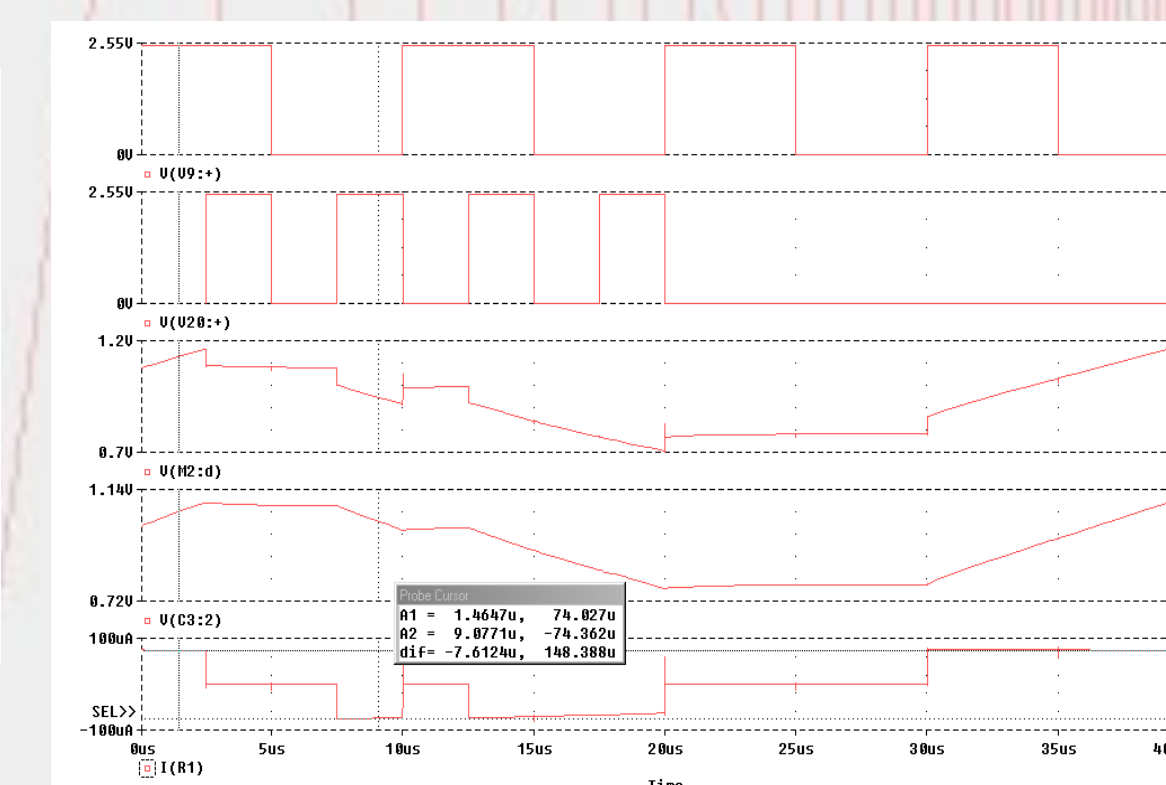
## Circuit Operation

- Phase Detector:** Creates an output proportional to the phase difference between its input signals, the incoming data and the feedback signal.
- Loop Filter:** A low pass filter; adds another pole to the feedback loop to control lock-in range and frequency.
- Voltage-Controlled Oscillator:** Produces a clock signal whose frequency is proportional to its input voltage.
- Divide-by-N Counter:** Feeds the output clock signal, its frequency divided by N, back to the PD.
- Closed Loop Gain:** 
$$H(s) = \frac{\Phi_{clock}}{\Phi_{data}} = \frac{K_{PD}K_{VCO}K_F}{s + \frac{1}{N}K_{PD}K_{VCO}K_F}$$

## Phase Detector & Loop Filter: Schematic and Responses

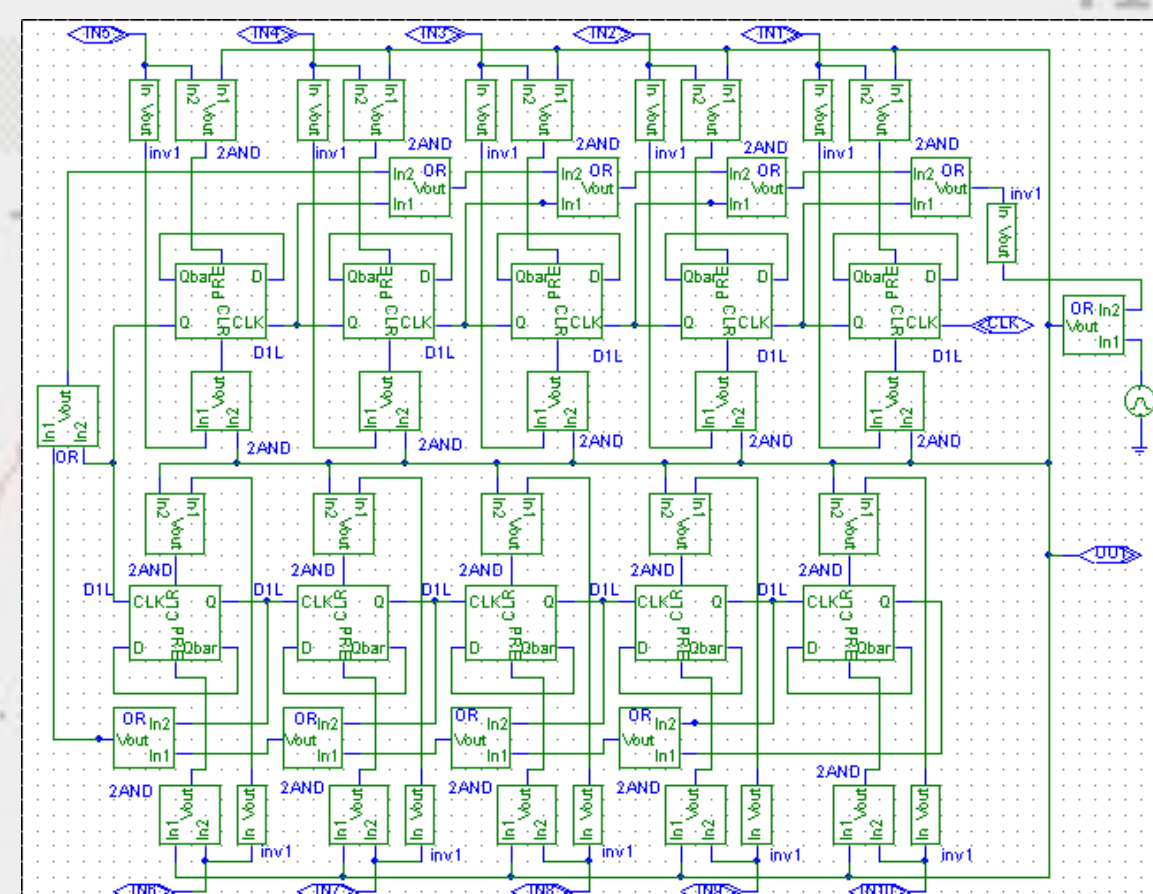


Phase detector and the loop filter

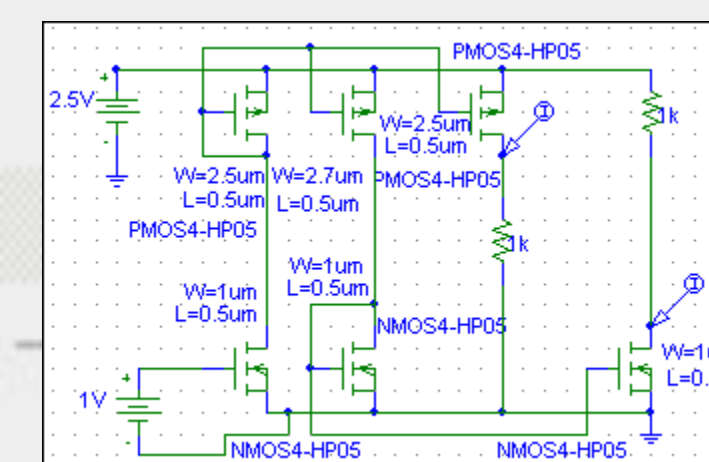


Transient responses for the phase detector and the loop filter

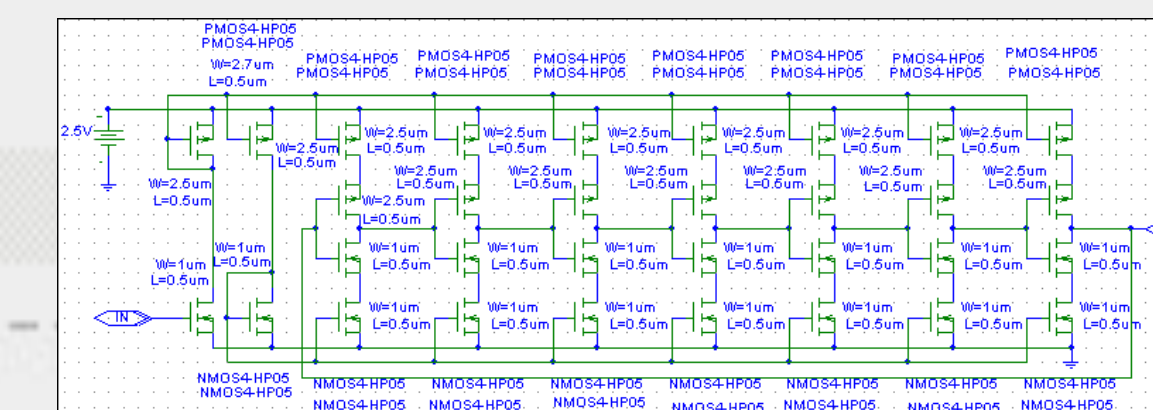
## 10-bit Counter Schematics



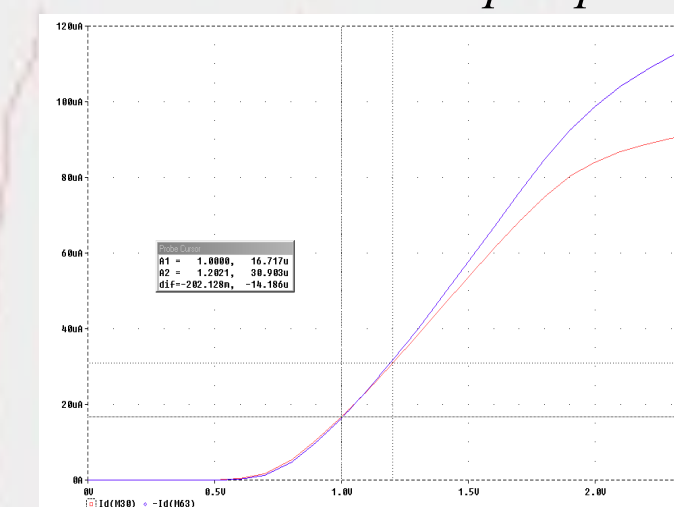
## VCO Current Pump and the VCO: Schematic and Responses



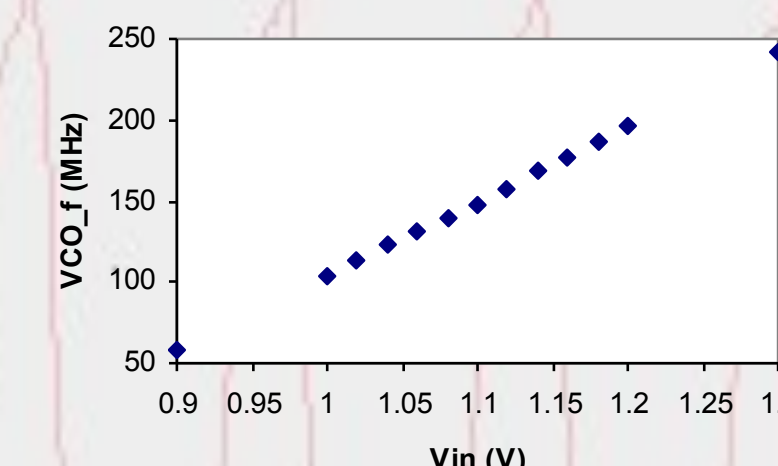
A VCO current pump



Full VCO

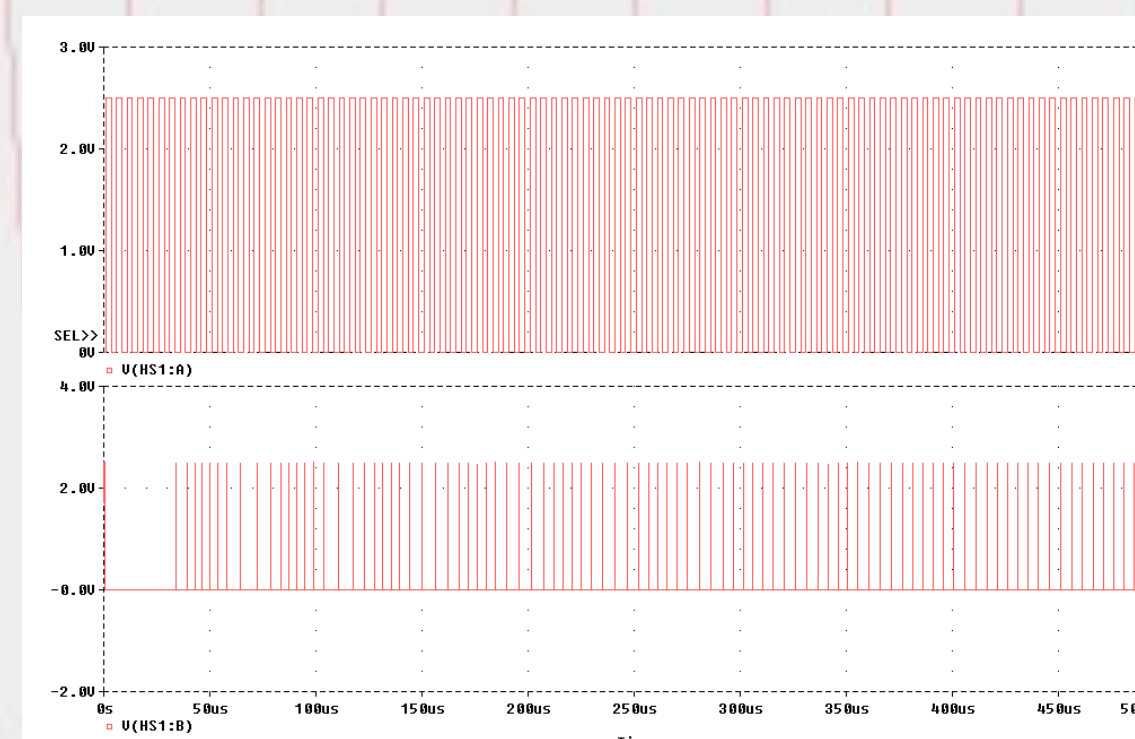


VCO current pump, current vs. V<sub>in</sub>

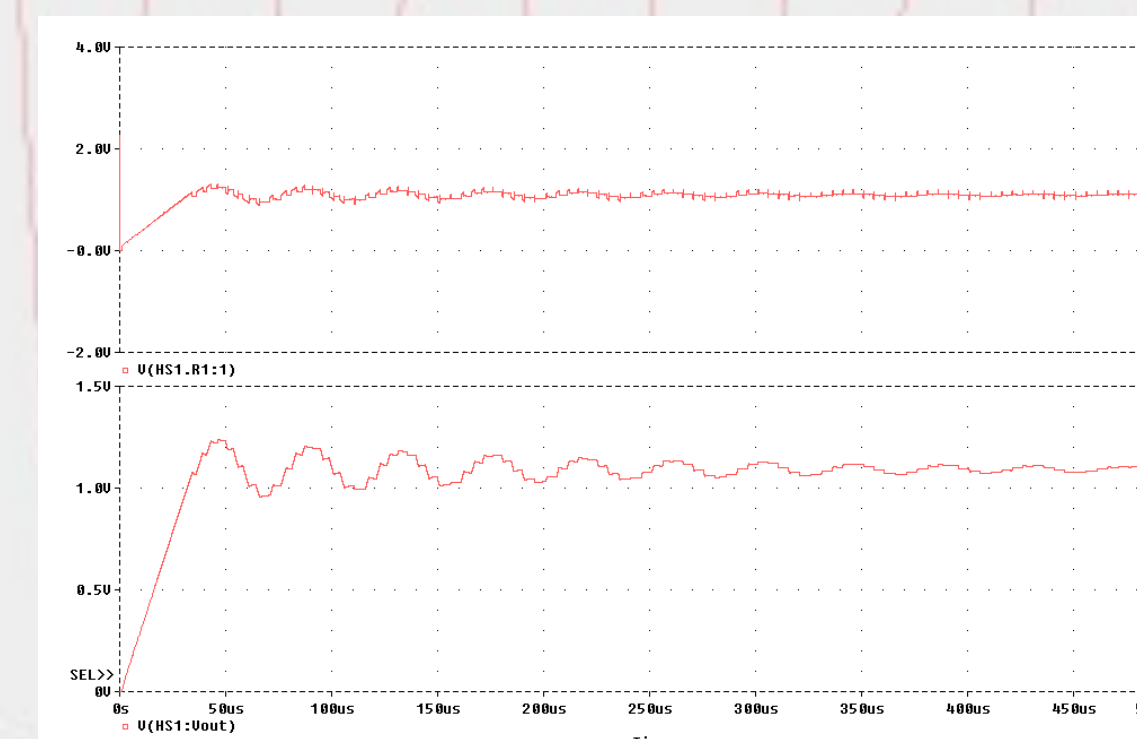


VCO, input voltage vs. frequency

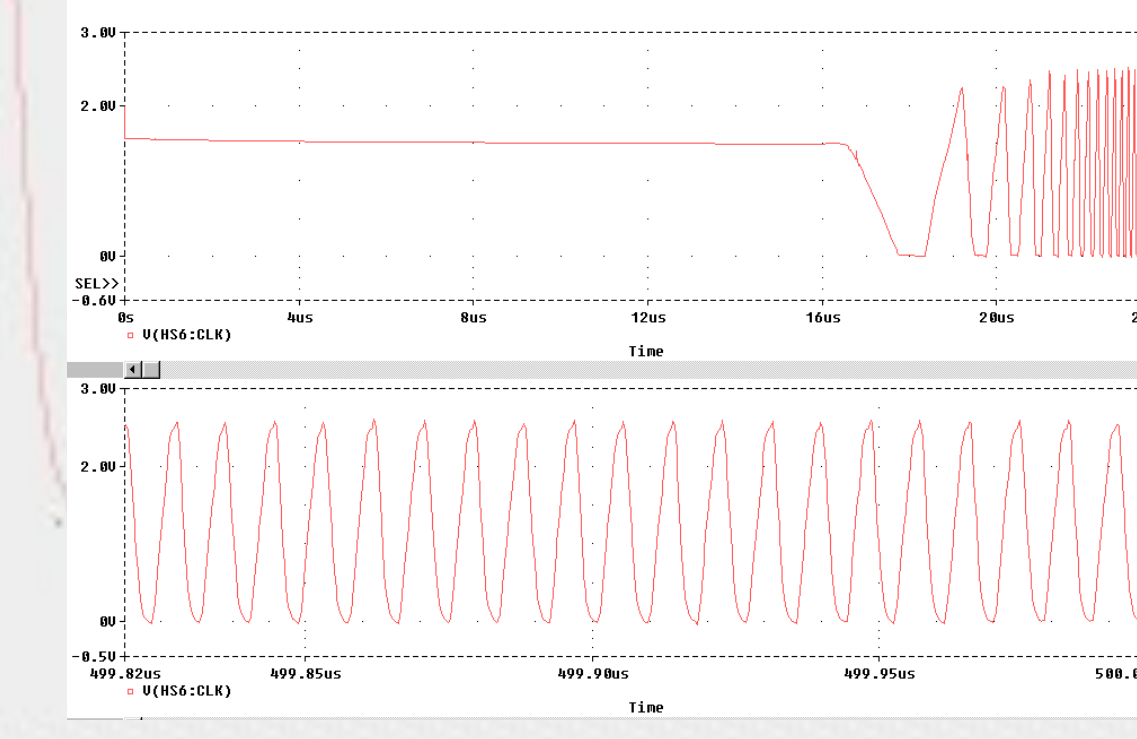
## Phase-Locked Loop, Operation: Simulation Results



Reference Clock and the Counter Output



PD output to loop filter and loop filter output to VCO



VCO outputs at the beginning of the simulation and after lock-in