A Low-Power Acoustic Periodicity Detector Chip for Voice and Engine Detection

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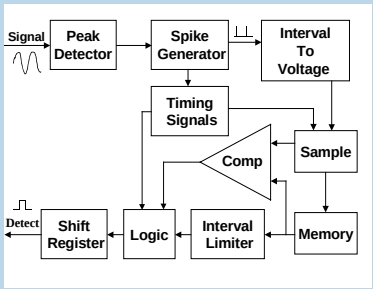
Introduction

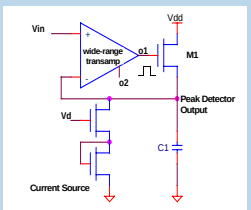
The detection of voices or the rumble of engines is a desirable function in many different devices from toys to smart homes to military applications. Typical approaches involving frequency-domain computation are quite computationally intensive and require a significant power and computational budget. In an effort to construct a very low-power detector capable of acting as a wake-up signal for other systems, we have designed a simple, low-power (1.5uW) analog VLSI circuit that **detects *periodicity in the time-domain envelope*** of the acoustic signal.

System Block Diagram

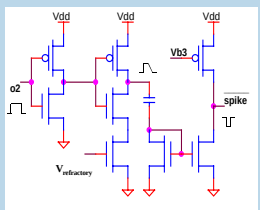


The circuit takes the input through a peak detector and generates a ***spike*** at the onset of a peak. The ***inter-spike intervals*** are then converted to a voltage. That voltage is then ***sampled*** and ***stored*** to be ***compared*** with the new sampled voltage. A *valid interval* that *matches* (as decided by the interval comparator stage) is called a ***hit***. The circuit can store up to five consecutive hits.

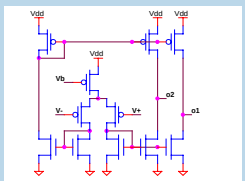
Peak Detector and Spike Generator Circuits



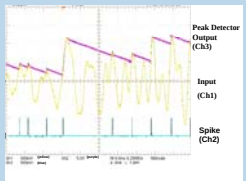
Peak detector: when peak detector's output drops below input, M1 is turned on charging C1 to Vin



Edge detector: the rising edge of o2 is used to generate a voltage spike.

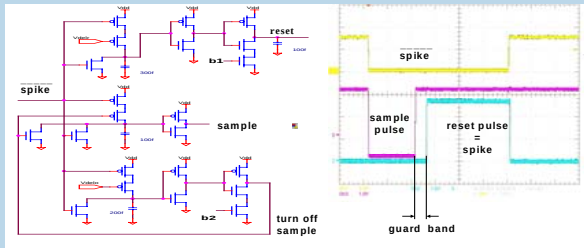


Dual-output, wide-range transconductance amplifier (transamp)



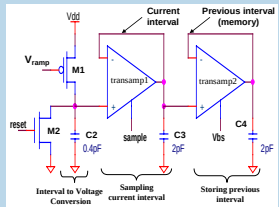
Oscilloscope trace demonstrates the peak detector's response to an input signal and the spike generation process

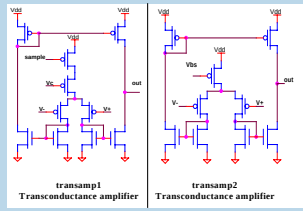
Circuit for Generating Timing Signals



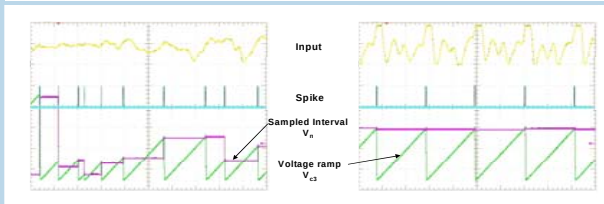
On the negative edge of $\overline{spike}$, three independent ramps are triggered with different slopes. As each ramp crosses the threshold of an inverter, a pulse is generated. The first ramp starts the sampling process by pulling the *sample* pulse low. The second ramp pulls *turn off sample* high, turning off the sampling pulse. The third ramp turns on the *reset* pulse. The guard interval can be adjusted to ensure that both the sampling process and the interval comparison have ended before the onset of the reset pulse.

Interval to Voltage Conversion, Sampling and Storing Intervals

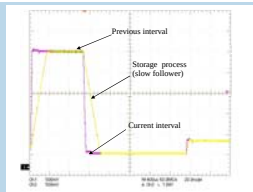




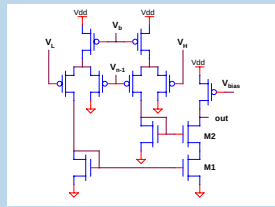
An inter-spike interval is linearly converted to a voltage by means of a voltage ramp. A voltage ramp is generated on C2 as it is being charged by a constant current source (M1). V_{ramp} controls the slope of the ramp. When a spike is triggered, two events take place; First, the voltage ramp V_{c2} is sampled when the sample pulse turns on the follower (transamp1). The ***sampled inter-spike interval V_n*** is temporarily stored on C3. Second, the reset pulse turns M2 on discharging C2 and the capacitor starts charging up again. The storage process occurs through a weakly biased follower (transmp2), this allows V_n to slowly be copied to C4 and stored as V_{n-1}.



Oscilloscope traces illustrate the interval-to-voltage conversion process by means of a voltage ramp, as well as the sampling and storing processes.

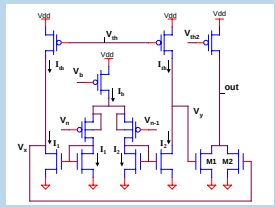


Interval Limiter



The interval limiter defines an acceptance zone defined in terms of voltages V_L and V_H. If the ***stored interval V_{n-1}*** satisfies the inequality $V_L<V_{n-1}<V_H$, then the two current mirrors will ensure that the two output transistors, M1 and M2, are on pulling the output of the circuit ***low indicating a valid interval***. If the inequality is not satisfied, one of the two output transistors will be off, the output will be pulled up ***high indicating an invalid interval***.

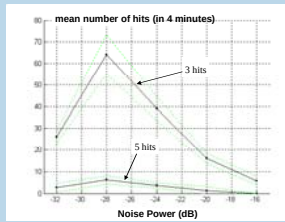
Interval Comparator



The interval comparator decides whether the two ***"inter-spike intervals"***, $\mathbf{V_n}$ and $\mathbf{V_{n-1}}$, ***match***. V_b sets a current I_b in the differential pair which is split into I_1 and I_2. V_{th} sets I_{th} such that $I_{th} < I_b/2$. When the two inputs match, both I_1 and I_2 are strong enough to hold V_x and V_y low turning off M1 and M2 and the ***output is high indicating matched intervals***. When the inputs do not match, one of the two output transistors, M1 and M2, is turned on pulling the ***output low indicating non-matching intervals***.

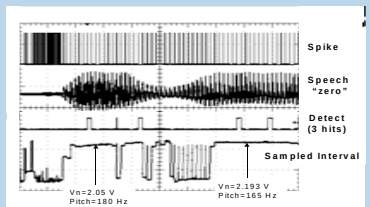
A ***valid interval*** together with ***matching intervals*** is defined as a ***hit***. Our chip can count up to five consecutive hits.

Chip Testing Results

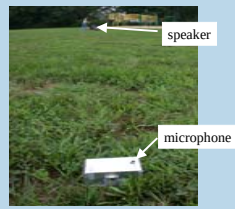


Chip response to a White Gaussian Noise input, lowpass filtered at 1KHz

Chip response to a 20 Hz sinusoidal input, lowpass filtered at 1 KHz



Response to the speech utterance "zero": No detection during the 'noisy' onset. Detects the voiced segments.The sampled interval can be used to estimate the pitch.



Chip being tested in the field

We thank Shihab Shamma for early discussions of this work and the Signal Systems Corporation for providing various acoustics recordings during the design period of this project. We also thank the MOSIS fabrication service for its continuous support in providing fabrication facilities. This work was supported by a contract with DARPA (Air Coupled Microsensors-0001400C0315)