Voltage Noise Induced DRAM Soft Error Reduction Technique for 3D CPUs

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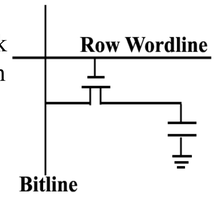
Background

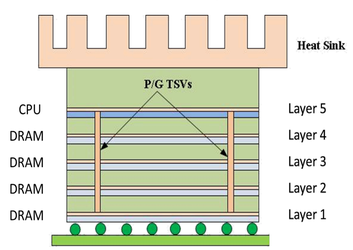
Soft Error in DRAM

- Voltage noise on DRAM wordline causes DRAM bit cells to leak
- Bit flip occurs when the accumulation (or deletion) of charges on the capacitors exceeds the noise margin
- Hard to correct or even detect multi-bit soft errors
- Previous work mainly focuses on soft error in DRAM induced by external particles



Soft Error in Stacked DRAM

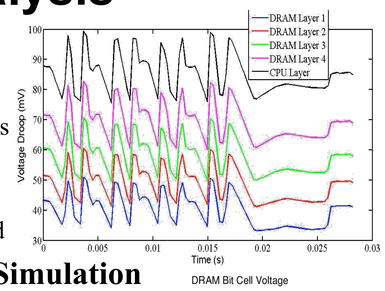
- CPU and DRAM share the power delivery network
- More severe thermal and voltage noise problems
- Strong voltage noise coupling between CPU and DRAM



Power and Thermal Analysis

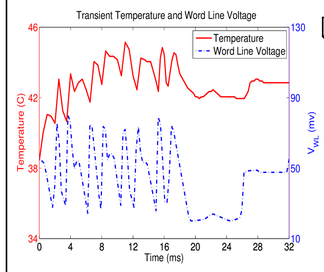
Power Delivery Analysis

- Strong coupling between DRAM and CPU
- Variance of bottom DRAM layer (DRAM layer 1) is smaller than that of CPU layer



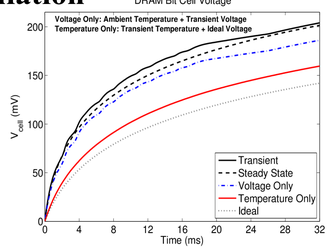
Thermal Analysis

- Temperature and voltage noise are highly correlated



DRAM SPICE Simulation

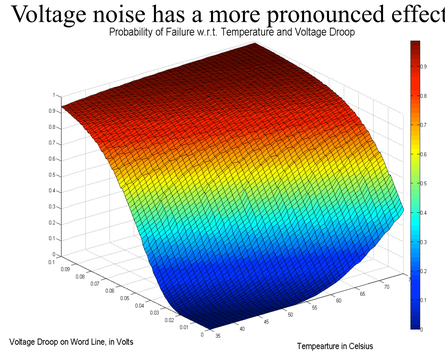
- Voltage noise has greater impact than temperature
- The steady state simulation converges with the real transient simulation at the end of the refresh cycle



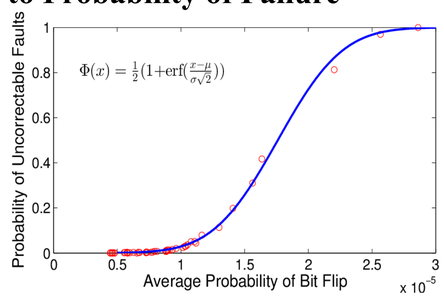
Reliability Analysis

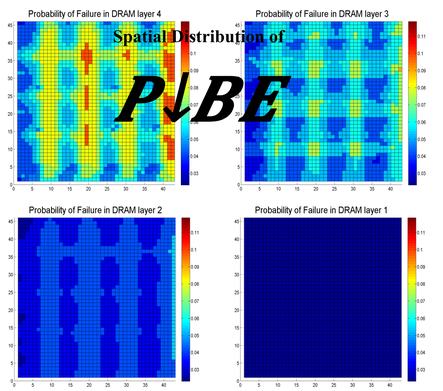
Probability of Bit Error (P_{BE})

- Perform Monte Carlo simulation to obtain DRAM bit cell's POF w.r.t. Temperature and wordline voltage
- Manufacturing randomness (oxide thickness) is considered
- Increasing voltage noise and temperature both increase P_{BE}
- Voltage noise has a more pronounced effect



Converting Bit Error Distribution to Probability of Failure

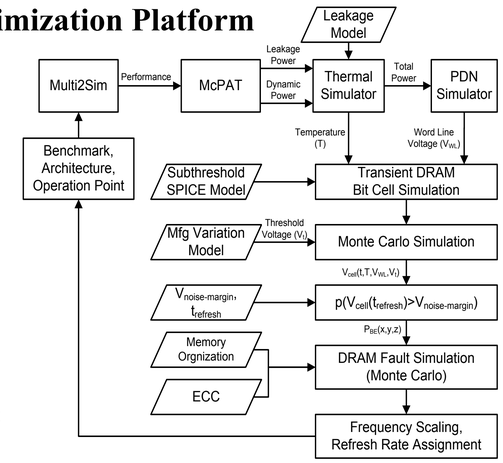




Dynamic Reliability Management

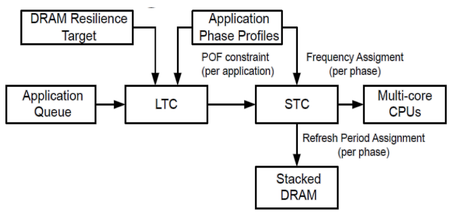
Co-simulation and Co-optimization Platform

- Multi-dimensional problem: performance, power, thermal, DRAM resilience etc.
- Multi-scale problem: performance transient (cycle-accurate) vs. DRAM resilience (long-term)
- Statistical problem: process variation



Dynamic Management

- Dynamic voltage and frequency scaling (DVFS)
- Dynamic refresh period adjustment



- **Optimization Goal**: maximize the system performance
- **Constraint: DRAM** resilience target (long-term probability of an uncorrectable memory error)

- **LTC:** Long-term controller determines at which operating point each **application** should be run to minimize runtime while meeting the long-term DRAM resilience
- **STC:** Short-term controller optimizes the runtime of each application by assigning an operating point to each **phase** of the application.
- **Observation:** an application with high power (high performance) may require frequency to be reduced, whereas a lower power application puts less stress on the DRAM resiliency and can be configured with a longer refresh period and get a performance boost

Simulation Results

Settings

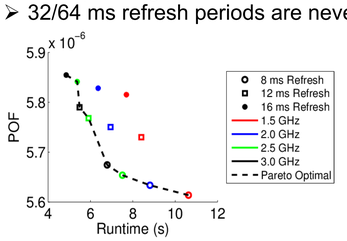
- **DRAM noise margin:** 10% V_{dd}
- **POF constraint:** 0.3%
- **LTC control window:** 30 minutes
- **Nominal case:** 3GHz clock rate + 8ms refresh period
- **Frequency selection:** {3.0, 2.5, 2.0, 1.5} GHz
- **Refresh period selection:** {8, 12, 16, 32, 64} ms

	Optimal	Nominal
Probability of uncorrectable error	0.30%	0.23%
Throughput(jobs/sec)	0.29	0.23
Normalized Throughput	1.27	1.00

Discussion

- Our controller improves performance in two ways
  1. Tradeoff resilience and performance
  2. Convert the slack in the POF to performance improvement
- Distribution of operating points

➢ The operating points that are not on the Pareto optimal from will never be chosen
➢ 32/64 ms refresh periods are never chosen due to fast bit flip



	Refresh Rate		
Frequency	8 ms	12 ms	16 ms
1.5GHz	1.8%	0.0%	0.0%
2.0GHz	1.8%	0.0%	0.0%
2.5GHz	7.2%	0.0%	0.5%
3.0GHz	59.3%	27.5%	2.0%

Conclusion

- We present a detailed analysis and optimization scheme for 3D CPUs on voltage noise induced DRAM transient fault
- We observe significant correlations between CPU activities and DRAM layer thermal and voltage noise
- We propose a dynamic DRAM management scheme in order to maximize performance while meeting long-term resilience target. Simulation results show that our management scheme achieves 27% increase in performance when comparing to running at the nominal operating point
- The work will be published in ISLEPD 2016

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